40

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,226	08/19/2003	Sivaram Krishnan	16869A-003510US	5724

20350 7590 03/27/2006

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
KIM, KENNETH S	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,226	KRISHNAN ET AL.	
	Examiner	Art Unit	
	Kenneth S. KIM	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

KENNETH S. KIM
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Sep22'03*. (Item 93 not received)
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 27-40 are presented for examination.

2. The abstract of the disclosure is objected to because the current abstract does not reflect the inventive feature of the claimed invention to distinguish over the prior art. Correction is required. See MPEP § 608.01(b).

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 27-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(a) Claim 27, 31, and 37, the limitation of the data length being equal to the instruction length appears to be an inappropriate recitation, since instruction length and data length are independent variables (and also not supported by the specification which describes an example of twice the length). One can have any data length regardless of the instruction length.

(b) Claims 29, 34, and 36, it is not clear what the pre-decode signal is used for. Merely calling an early portion of a unit a pre-unit does not add patentable limitation.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 27-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Jaggar, U.S. Patent No. 5,568,646.

Jaggar teaches the invention as claimed in claim 27 including a data processing unit comprising:

(a) an instruction cache to store instructions for execution, including instructions belonging to an M-bit instruction set and instructions belonging to an N-bit instruction set, where M < N (4, col. 4, lines 10-13)

(b) an instruction fetch unit coupled to receive instructions from the instruction cache, and operable to produce control signals representative of decoded N-bit instructions (18, 22, 24; col. 4, line 11),

(c) one or more execution units coupled to the receive the control signals from the instruction fetch unit (8,10,12)

(d) the instruction fetch unit comprising a translation unit to translate an M-bit instruction received from the instruction cache to produce one or more N-bit instructions (38, 40; col. 4, line 62)

(e) the instruction fetch unit further comprising a decoder unit to decode only N-bit instructions, thereby producing the control signals, the translation unit configured to deliver the one or more N-bit instructions to the decoder unit (32; col. 4, line 63)

(f) wherein the M-bit instruction set includes data instructions that produce M-bit results, wherein the N-bit instruction set includes first data instructions that produce N-bit results and second data instructions that produce M-bit results (can be any length result),

(g) wherein the instruction fetch unit is configured to produce one or more of the second data instructions in response to receiving an M-bit data instruction (col. 4, line 63), and

further teaches as in claims 28-30,

(h) store the M-bit results into an N-bit data store and perform sir-extension of the M-bit result in the N-bit data store to produce an N-bit result (to match the data length) – claim 28,

(i) the instruction fetch unit includes a pre-decoder unit (38 or pipeC) configured to receive N-bit instructions from the instruction cache and to produce one or more pre-decode signals in response to a received N-bit instruction, the pre-decoder unit providing a signal path to deliver the received N-bit instruction and the one or more pre-decode signals to the decoder, wherein the translation unit is further configured to produce corresponding pre-decode signals associated with the one or more N-bit instructions and to deliver the corresponding pre-decode signals to the decoder, wherein the corresponding pre-decode signals are pre-decode signals that would be produced if the one or more N-bit instructions were processed by the pre-decoder unit (38 is used as pre-decoder as well as part of the translator) – claim 29, and

(j) M is 16, and N is 32 (can be any set of numbers) – claim 30.

The processor claims 31-35 and the microprocessor claims 36-40 are equivalently rejected based on the same reason.

7. Claims 27-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Hammond et al, U.S. Patent No. 5,638,525, cited by the applicant.

Hammond et al teaches the invention as claimed in claim 27 including a data processing unit comprising:

(a) an instruction cache to store instructions for execution, including instructions belonging to an M-bit instruction set and instructions belonging to an N-bit instruction set, where M < N (642, col. 4, line 57)

(b) an instruction fetch unit coupled to receive instructions from the instruction cache, and operable to produce control signals representative of decoded N-bit instructions (640, 641, 643; col. 16, line 24),

(c) one or more execution units coupled to the receive the control signals from the instruction fetch unit (644)

(d) the instruction fetch unit comprising a translation unit to translate an M-bit instruction received from the instruction cache to produce one or more N-bit instructions (641; col. 16, line 22)

(e) the instruction fetch unit further comprising a decoder unit (643) to decode only N-bit instructions, thereby producing the control signals, the translation unit configured to deliver the one or more N-bit instructions to the decoder unit (col. 16, line 22)

(f) wherein the M-bit instruction set includes data instructions that produce M-bit

results, wherein the N-bit instruction set includes first data instructions that produce N-bit results and second data instructions that produce M-bit results (can be any length result),

(g) wherein the instruction fetch unit is configured to produce one or more of the second data instructions in response to receiving an M-bit data instruction (col. 16, line 44), and

further teaches as in claims 28-30,

(h) store the M-bit results into an N-bit data store and perform sir-extension of the M-bit result in the N-bit data store to produce an N-bit result (to match the data length) – claim 28,

(i) the instruction fetch unit includes a pre-decoder unit (early stage of decoder redundant in translator later stage) configured to receive N-bit instructions from the instruction cache and to produce one or more pre-decode signals in response to a received N-bit instruction, the pre-decoder unit providing a signal path to deliver the received N-bit instruction and the one or more pre-decode signals to the decoder, wherein the translation unit is further configured to produce corresponding pre-decode signals associated with the one or more N-bit instructions and to deliver the corresponding pre-decode signals to the decoder, wherein the corresponding pre-decode signals are pre-decode signals that would be produced if the one or more N-bit instructions were processed by the pre-decoder unit (redundant features generate the same signals) - claim 29, and

(j) M is 16, and N is 32 (can be any set of numbers) – claim 30.

The processor claims 31-35 and the microprocessor claims 36-40 are equivalently rejected based on the same reason.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sites et al taught a method of sign extending to match data length for different data length instructions (col. 17, lines 2-7).

Arya taught a method on converting instructions for execution in new architecture.

Borrill taught a method of execution multiple instruction sets.

Hookway et al taught a method of sign extending to match data length (col. 85, line 27).

9. Applicant is reminded that item 93 in the submitted prior art list has not been received.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth S KIM whose telephone number is (571) 272-3627. The examiner can normally be reached on M-F (8:30-17:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for all communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

KENNETH S. KIM
PRIMARY EXAMINER